CLAIMS

1. An external storage device comprising:

a system interface section for conducting interface with a host computer;

a first memory storage area and a second memory storage area for storing sector data;

error correcting means for performing error detection and error correction for said sector data; and

control means for controlling a reading and writing operation of sector data with respect to said first memory storage area and said second memory storage area;

wherein in response to a write command from said host computer, said control means stores a plurality of sector data pertaining to said write command in sector units alternately in said first memory storage area and said second memory storage area, and

in response to a read command from said host computer, said control means reads out a first sector data among a plurality of sector data required by the read command from one of said first memory storage area and said second memory storage area, and supplies a read-out sector data to said error correcting means, and then said control means reads out sector data of said first memory storage area and said second memory storage area simultaneously, so that while N-th (where N is a natural number) sector data from one of said first memory storage area and said second memory storage area are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

2. An external storage device as set forth in claim 1, wherein said data changing means has a first arrangement for selectively connecting sector data from said first memory storage area to either of said system interface section and said error correcting means and a second arrangement for selectively connecting sector data from said second memory storage area to an opposite one of said system interface section and said error correcting means, and said control means controls alternate read-out of sector data from said first memory storage area and said second memory storage area by changing said data changing means to alternately connect sector data from said first memory storage area and said second memory storage area to said system interface section during sequential read-out clock cycles.

3. An external storage device as set forth in claim 1, further comprising a write buffer for temporarily storing write sector data from said host computer, wherein the write sector data are stored to said first memory storage area and said second memory storage area through said write buffer.

4. An external storage device as claimed in claim 1, wherein during a first-out read clock cycle following the read command, said control means is arranged to read out said first sector data, and for a second and subsequent read-out clock cycles following the read command, said control means reads out sector data of said first memory storage area and said second memory storage area simultaneously, so that while the N-th (where N is a natural number) sector data from one of said first memory storage area and said second memory storage area are transferred to said

system interface section, the (N + 1)th sector data from the other are transferred to said error correcting means.

5. An external storage device as claimed in claim 1, wherein said control means has an arrangement which, upon detection of data error by said error correcting means, temporarily interrupts the simultaneous read-out of sector data of said first memory storage area and said second memory storage area to allow error correction, and allows continued simultaneous read-out of sector data of said first memory storage area and said second memory storage area only upon determination of no error correction or completion of error correction.

6. An external storage device as claimed in claim 1, wherein said error correcting means has a data bit throughput which is greater than that of a bus width of a system bus connecting said system interface section and said host computer.

7. An external storage device as claimed in claim 1, wherein said first memory storage area provided by and said second memory storage area are discrete static storage devices each having a memory bus width which is the same as a bus width of a system bus.

8. An external storage device as claimed in claim 1, wherein said first memory storage area and said second memory storage area are opposite ones of upper and lower storage bits within a single static storage device having a memory bus width which is greater than a bus width of a system bus.

9. An external storage device comprising:

a system interface section for conducting interface with a host computer;

a memory for storing sector data, and having a memory bus with a memory bus width which is twice a width of a system bus;

error correcting means for performing error detection and error correction for said sector data; and

control means for controlling a reading and writing operation of sector data with respect to said memory;

wherein in response to a write command from said host computer, said control means stores odd-numbered sector data pertaining to the write command in memory locations accessed by one of an upper side and a lower side of said memory bus, and also stores even-numbered sector data pertaining to the write command in memory locations accessed by an opposite one of said upper side and said lower side of said memory bus, and

in response to a read command from said host computer, said control means reads out a first sector data among a plurality of sector data required by the read command using one of said upper side and said lower side of said memory bus, and supplies a read-out sector data to said error correcting means, and then said control means reads out sector data using both of said upper side and said lower side of said memory bus simultaneously, so that while N-th (where N is a natural number) sector data from one of said upper side and said lower side of said memory bus are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

10. An external storage device as set forth in claim 9, wherein said data changing means has a first arrangement for selectively connecting sector data from said upper side of said memory bus to either of said system interface section and said error correcting means and a second arrangement for selectively connecting sector data from said lower side of said memory bus to an opposite one of said system interface section and said error correcting means, and said control means controls alternate read-out of sector data from said upper side and said lower side of said memory bus by changing said data changing means to alternately connect sector data from said upper side and said lower side of said memory bus to said system interface section during sequential read-out clock cycles.

11. An external storage device as set forth in claim 9, further comprising a write buffer for temporarily storing write sector data from said host computer, wherein the write sector data are stored to said memory through said write buffer.

12. An external storage device as claimed in claim 9, wherein during a first read-out clock cycle following the read command, said control means is arranged to read out said first sector data, and for a second and subsequent read-out clock cycles following the read command, said control means reads out sector data using both of said upper side and said lower side of said memory bus simultaneously, so that while N-th (where N is a natural number) sector data from one of said upper side and said lower side of said memory bus are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

13. An external storage device as claimed in claim 9, wherein said control means has an arrangement which, upon detection of data error by said error correcting means, temporarily interrupts the simultaneous read-out of sector data of both said upper side and said lower side of said memory bus to allow error correction, and allows continued simultaneous read-out of sector data of said upper side and said lower side of said memory bus only upon determination of no error correction or completion of error correction.

14. An external storage device as claimed in claim 1, wherein said error correcting means has a data bit throughput which is greater than that of a bus width of a system bus connecting said system interface section and said host computer.

15. A memory access control method of an external storage device having:

a system interface section for conducting interface with a host computer;

a first memory storage area and a second memory storage area for storing sector data;

error correcting means for performing error detection and error correction for said sector data; said method comprising the steps of:

storing, in response to a write command from a host computer, a plurality of sector data pertaining to said write command in sector units alternately in said first memory storage area and said second memory storage area; and

reading, in response to a read command from said host computer, a first sector data among a plurality of sector data required by the read command from one of said first memory storage area and said second memory storage area, and supplying a read-out sector data to said error correcting means, and then reading out

sector data of said first memory storage area and said second memory storage area simultaneously, so that while N-th (where N is a natural number) sector data from one of said first memory storage area and said second memory storage area are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

16. A method as set forth in claim 15, wherein said data changing means has a first arrangement for selectively connecting sector data from said first memory storage area to either of said system interface section and said error correcting means and a second arrangement for selectively connecting sector data from said second memory storage area to an opposite one of said system interface section and said error correcting means, and said method further includes a step of controlling alternate read-out of sector data from said first memory storage area and said second memory storage area by changing said data changing means to alternately connect sector data from said first memory storage area and said second memory storage area to said system interface section during sequential read-out clock cycles.

17. A method as set forth in claim 15, further comprising a write buffer for temporarily storing write sector data from said host computer, wherein during said writing step, the write sector data are stored to said first memory storage area and said second memory storage area through said write buffer.

18. A method as claimed in claim 15, wherein said reading step reads out said first sector data during a first read-out clock cycle following the read command,

and for a second and subsequent read-out clock cycles following the read command, reads out sector data of said first memory storage area and said second memory storage area simultaneously, so that while the N-th (where N is a natural number) sector data from one of said first memory storage area and said second memory storage area are transferred to said system interface section, the (N + 1)th sector data from the other are transferred to said error correcting means.

19. A method as claimed in claim 15, wherein, upon detection of data error by said error correcting means, said reading step temporarily interrupts the simultaneous read-out of sector data of said first memory storage area and said second memory storage area to allow error correction, and allows continued simultaneous read-out of sector data of said first memory storage area and said second memory storage area only upon determination of no error correction or completion of error correction.

20. A method as claimed in claim 15, wherein said error correcting means has a data bit throughput which is greater than that of a bus width of a system bus connecting said system interface section and said host computer.

21. A method as claimed in claim 15, wherein said first memory storage area and said second memory storage area are provided by discrete static storage devices each having a memory bus width which is the same as a bus width of a system bus.

22. A method as claimed in claim 15, wherein said first memory storage area and said second memory storage area are opposite ones of upper and lower storage bits within a single static storage device having a memory bus width which is greater than a bus width of a system bus.

23. A memory access control method of an external storage device having:

a system interface section for conducting interface with a host computer;

a memory for storing sector data, and having a memory bus with a memory bus width which is twice a width of a system bus;

error correcting means for performing error detection and error correction for said sector data; said method comprising the steps of:

storing, in response to a write command from a host computer, odd-numbered sector data pertaining to the write command in memory locations accessed by one of an upper side and a lower side of said memory bus, and even-numbered sector data pertaining to the write command in memory locations accessed by an opposite one of said upper side and said lower side of said memory bus; and

reading, in response to a read command from said host computer, a first sector data among a plurality of sector data required by the read command using one of said upper side and said lower side of said memory bus, and supplying a read-out sector data to said error correcting means, and then reading out sector data using both of said upper side and said lower side of said memory bus simultaneously, so that while N-th (where N is a natural number) sector data from one of said upper side and said lower side of said memory bus are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

24. An external storage device as set forth in claim 23, wherein said data changing means has a first arrangement for selectively connecting sector data from said upper side of said memory bus to either of said system interface section and said error correcting means and a second arrangement for selectively connecting sector data from said lower side of said memory bus to an opposite one of said system interface section and said error correcting means, and said method further includes a step of controlling alternate read-out of sector data from said upper side and said lower side of said memory bus by changing said data changing means to alternately connect sector data from said upper side and said lower side of said memory bus to said system interface section during sequential read-out clock cycles.

25. An external storage device as set forth in claim 23, further comprising a write buffer for temporarily storing write sector data from said host computer, wherein during said writing step, the write sector data are stored to said memory through said write buffer.

26. An external storage device as claimed in claim 23, wherein said reading step reads out said first sector data during a first read-out clock cycle following the read command, and for a second and subsequent read-out clock cycles following the read command, reads out sector data using both of said upper side and said lower side of said memory bus simultaneously, so that while N-th (where N is a natural number) sector data from one of said upper side and said lower side of said memory bus are transferred to said system interface section, (N + 1)th sector data from the other are transferred to said error correcting means.

27. An external storage device as claimed in claim 23, wherein, upon detection of data error by said error correcting means, said reading step temporarily interrupts the simultaneous read-out of sector data of both said upper side and said lower side of said memory bus to allow error correction, and allows continued simultaneous read-out of sector data of said upper side and said lower side of said memory bus only upon determination of no error correction or completion of error correction.

28. An external storage device as claimed in claim 23, wherein said error correcting means has a data bit throughput which is greater than that of a bus width of a system bus connecting said system interface section and said host computer.